REMARKS

Reconsideration of the application in view of the above amendments and the following remarks is requested. Claims 3, 5, 8-9, 12, 14, 17-20, 23-26, 28-33, and 37-40 are in this application. Claims 1-2, 4, 6-7, 10-11, 13, 15-16, 21-22, 27, and 34-36 have been cancelled. Claims 25-26 and 28-33 have been amended. Claims 37-40 have been added to alternately and additionally claim the present invention. In addition to the amendments discussed below, claims 25-26 and 28-33 have been significantly amended to more clearly recite and alternately claim the present invention. These amendments were not made for reasons of patentability.

The Examiner rejected claims 25-29 and 32-35 under 35 U.S.C. §102(b) as being anticipated by Hmida (U.S. Patent No. 4,920,509). For the reasons set forth below, applicant respectfully traverses this rejection.

Claim 25 has been amended, and recites, in part:

> "a first output circuit having:
>
> "a first transmission gate having first and second transistors connected to an input and an output, the first and second transistors having first and second gates, respectively;
>
> "a second transmission gate having first and second transistors connected to an input and an output, the first and second transistors of the second transmission gate having first and second gates, respectively, the outputs of the first and second transmission gates being connected together;
>
> "a third transmission gate having first and second transistors connected to an input and an output, the first and second transistors of the third transmission gate having first and second gates, respectively;
>
> "a fourth transmission gate having first and second transistors connected to an input and an output, the first and second transistors of the fourth transmission gate having first and second gates, respectively, the outputs of the third and fourth transmission gates being connected together; and
>
> "a first inverting circuit having an input connected to the input of the second transmission gate and the input of the third transmission gate, and an output connected to the input of the fourth transmission gate."

In rejecting the claims, the Examiner pointed to transmission gates C1-C4 shown in FIG. 1 of Hmida as constituting the first output circuit required by claim 25, and inverter I4 shown in FIG. 1 of Hmida as constituting the first inverting circuit required by claim 25. Transmission gates C1-C4, however, can not be read to be the transmission gates required by amended claim 25.

As noted above, claim 25 requires that the first inverting circuit have an input that is connected to the inputs of the second and third transmission gates. However, as shown in FIG. 1 of Hmida, the input of inverter I4 is connected to the input of only one transmission gate, namely the input of transmission gate C2. As a result, the input of inverter I4 is not connected to the inputs of both the second and third transmission gates as required by claim 25.

Thus, since the input of inverter I4 is not connected to the inputs of both the second and third transmission gates, amended claim 25 is not anticipated by the Hmida reference. In addition, since claims 26, 28-29, 32-33, and new claims 37-40 depend either directly or indirectly from claim 25, claims 26, 28-29, 32-33, and 37-40 are not anticipated by claim 25 for the same reasons as claim 25. (Claims 27 and 34-35 have been cancelled.)

The Examiner rejected claims 3, 5, 8-9, 12, 14, 17, 23-24, 30-31, and 36 under 35 U.S.C. §103(a) as being unpatentable over Hmida. For the reasons set forth below, applicant respectfully traverses this rejection.

Claim 3 recites, in part:

> "a first logic gate having a first input that receives a first input signal, a second input that receives a second input signal, and a first output that generates a first logic signal, the first input signal, the second input signal, and the first logic signal each having a logic state, the first logic gate generating the first logic signal in response to the logic states of the first and second input signals, the first logic gate generating an inverted first input signal in response to the first input signal;
>
> "a first carry out circuit having a first control input connected to receive the first logic signal, a second control input connected to receive the inverted first logic signal, and an output, the carry out circuit including a first

multiplexer that passes a first received signal to the output of the first carry out circuit when the first logic signal has a first logic state, and passes a second received signal to the output of the first carry out circuit when the first logic signal has a second logic state, the first received signal being the first input signal."

In rejecting the claims, the Examiner pointed to exclusive OR gate XOR1 or XOR2 shown in FIG. 1 of Hmida as constituting the first logic gate required by claim 3, and transmission gates C3-C4 shown in FIG. 1 of Hmida as constituting the first carry out circuit required by claim 3. With regard to the requirement that the first received signal be the first input signal, the Examiner acknowledged that Hmida does not teach this limitation.

With regard to the missing limitation, the Examiner argued that it would be obvious to modify the adder shown in FIG. 1 of Hmida to provide the necessary connection. The Examiner first argued that FIG. 1 of Hmida teaches that the first received signal is an inverted first input signal. If the signal input to transmission gate C3 is read to be the first received signal, and the input signal Ai is read to be the first input signal, then the first received signal can be read to be an inverted first input signal.

The Examiner next argued that it would be a simple modification to the adder circuit shown in FIG. 1 of Hmida to use the first input signal rather than the inverted first input signal. The Examiner then pointed to applicant's teachings and claims (page 18, lines 12-19, FIGS. 3, 6, and 9, and claim 4) as support for the argument that it would be a simple modification.

Following this, the Examiner appears to argue that one skilled in the art would be motivated to modify the adder shown in FIG. 1 of Hmida (so that the first input signal is used rather than the inverted first input signal) to design the claimed invention according to Hmida's teachings because the device is a full adder cell as claimed. (Although not required by claim 3, FIG. 1 of Hmida would require additional modifications beyond the inverter connection to realize the circuit.)

Applicant notes that to establish a prima facia case of obviousness, the Examiner must set forth a reason why one skilled in the art would be motivated to make the changes suggested by the Examiner. Applicant respectfully does not understand the Examiner's statement of motivation, which appears to be that if one skilled in the art were in the possession of Hmida's FIG. 1 adder, and were tasked to design an adder that responded to different signal polarities, one skilled in the art would be motivated to modify Hmida's FIG. 1 adder because Hmida's FIG. 1 adder is a full adder cell.

The needed motivation, however, is not an event that would motivate a person into action (such as a request to satisfy a design desire), but instead must come from a prior art teaching or knowledge generally held in the art that suggests making the specific change. From what applicant can determine, the Examiner has not identified any teaching in Hmida that suggests how to modify Hmida's FIG. 1 adder to respond to different signal polarities. Further, the Examiner has not indicated why one skilled in the art would be motivated to modify Hmida's FIG. 1 adder as opposed to any other adder.

With respect to applicant's teaching in the specification that an adder cell can be changed to respond to different signal polarities by simply reconnecting a few wires, this teaching is merely an indication of the difficulty in implementing different aspects of the invention. Implementation difficulty, however, is not a standard of obviousness. Inventions are not measured by how easy or difficult the inventions are to implement, but whether one skilled in the art would be motivated to make the invention in view of the prior art. Further, applicant can find nothing in FIGS. 3, 6, and 9 which suggests obviousness.

With respect to applicant's alternate claiming in original claims 3 and 4, alternate claiming can not be read to mean that the two different circuits recited by claims 3 and 4 are obvious in view of each other. For example, when two species claims depend from a genus claim, the two species claims are not considered to be obvious in view of each other.

The issue is not how difficult it is to transform one circuit into another, or what would motivate a person into action (such as a request to satisfy a design desire), but instead is whether or not there is a prior art teaching that suggests making the specific change. The Examiner does not appear to have pointed to any prior art teaching, or knowledge generally held in the art, that would suggest making the change to one skilled in the art.

Thus, from what applicant can determine, the Examiner has not set forth a prima facia case of obviousness. As a result, claims 3, 5, 8-9, 12, 14, 17, 23-24, 30-31, and 36 are patentable over Hmida.

With further respect to claim 17, this claim recites a second adder cell where the active states of the outputs of the carry out circuits of the first and second adder cells are opposite. In rejecting the claims, the Examiner pointed to FIG. 5 of Hmida as teaching two adder cells. However, neither of the two adder cells shown in FIG. 5 of Hmida is the adder cell shown in FIG. 1 of Hmida. Thus, FIG. 5 of Hmida appears to suggest the use of two adder cells.

However, if two adder cells from FIG. 1 of Hmida were connected together, applicant can find nothing that teaches or suggests that the active states of the outputs of the carry out circuits of the first and second adder cells would be opposite. From what applicant can determine, if two of Hmida's FIG. 1 adder cells were connected together, the outputs of both cells would have the same active state. Thus, claim 17 is patentable over Hmida for this additional reason.

The Examiner rejected claims 18-20 under 35 U.S.C. §103(a) as being unpatentable over Hmida in view of Mazin et al. (U.S. Patent No. 4,866,658). In rejecting the claims, the Examiner appears to point to the discussion of Hmida as teaching the use of two adder cells, and Mazin as teaching the use of three adder cells that can lie in different rows.

However, as just noted, from what applicant can determine, the Hmida reference does not teach or suggest the use of two FIG. 1 adder cells which have outputs with opposite active states. As a result, claims 18-20, which depend either

directly or indirectly from claim 17, are patentable over Hmida in view of Mazin for the same reasons that claim 17 patentable over Hmida.

Thus, for the foregoing reasons, it is submitted that all of the claims are in a condition for allowance. Therefore, the Examiner's early re-examination and reconsideration are respectively requested.

Respectfully submitted,

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